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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.								
10/694,477	10/27/2003	Shunpei Yamazaki	0553-0118.01	4264								
<div>7590 08/29/2007 Edward D. Manzo Cook, Alex, McFarron, Manzo, Cummings &amp; Mehler, Ltd. 200 West Adams St., Ste. 2850 Chicago, IL 60606</div>			<div>EXAMINER PRENTY, MARK V</div> <table border="1"><thead><tr><th>ART UNIT</th><th>PAPER NUMBER</th></tr></thead><tbody><tr><td>2822</td><td></td></tr></tbody></table> <table border="1"><thead><tr><th>MAIL DATE</th><th>DELIVERY MODE</th></tr></thead><tbody><tr><td>08/29/2007</td><td>PAPER</td></tr></tbody></table>		ART UNIT	PAPER NUMBER	2822		MAIL DATE	DELIVERY MODE	08/29/2007	PAPER
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/694,477

Applicant(s)

YAMAZAKI, SHUNPEI

Examiner

MARK PRENTY

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 20 August 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) See Continuation Sheet is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 39, 41, 43, 44, 46, 48, 49, 51, 53, 57-65, 69-84 and 87 is/are allowed.
- 6) ☒ Claim(s) 24, 25, 28-30, 33-35, 38 and 54-56 is/are rejected.
- 7) ☒ Claim(s) 86 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application
- ☐ Other: \_\_\_\_\_

Continuation of Disposition of Claims: Claims pending in the application are 24,25,28-30,33-35,38,39,41,43,44,46,48,49,51,53-65,69-84,86 and 87.

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This Office Action is in response to the amendment filed on August 20, 2007.

Claim 86 is objected to because "the pair of the impurity regions" lacks antecedent basis. Correction is required (it should read "the three impurity regions").

Claims 54-56 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, claims 54-56 are indefinite because "the semiconductor film" lacks antecedent basis and because on the whole they are inconsistent with their amended independent claims' "semiconductor substrate" context.

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 4,004,159 to Rai et al. (Rai) together with United States Patent 5,885,872 to Tamaki et al. (Tamaki, already of record).

As to independent claim 24, Rai discloses a semiconductor device (see the entire patent, including the Fig. 3 disclosure) comprising: a semiconductor substrate 1; a pair of first impurity regions 2, 3 being formed in the semiconductor substrate; an active region formed between the pair of first impurity regions in the semiconductor substrate; a floating gate 5 formed over and insulated from the active region; and a control gate 7 formed over and insulated from the floating gate.

The difference between claim 24 and Rai is claim 24 further comprises: "at least two second impurity regions formed in said semiconductor substrate between the pair of first impurity regions; at least one channel region between the at least two second impurity regions; boundaries between the channel region and the at least two second impurity regions extending in a direction along a carrier flow direction of the channel

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region...wherein the floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the at least two second impurity regions.”

Tamaki teaches providing a transistor with two impurity regions extending from the source region to the drain region to control the transistor's channel width and thus its conductance (see the entire patent, including the Fig. 5 disclosure).

It would have been obvious to one skilled in this art to provide Rai's transistor with two (second) impurity regions extending from source region 2 to drain region 3 (resulting in a semiconductor device whose floating gate overlaps a boundary between at least one of the pair of the first impurity regions and the two second impurity regions) to control the transistor's channel width and thus its conductance as taught by Tamaki.

Claim 24 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki.

As to dependent claim 25, Tamaki's impurity regions 9 have a striped shape.

Claim 25 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki.

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 4,004,159 to Rai et al. (Rai) together with United States Patent 5,885,872 to Tamaki et al. (Tamaki, already of record) and United States Patent 5,936,887 to Choi et al. (Choi).

Claim 28 depends on independent claim 24, which is rejected under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki (see above). The above explanation of the rejection of independent claim 24 under 35 U.S.C. 103(a) as being

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unpatentable over Rai together with Tamaki is hereby incorporated by reference into this rejection of dependent claim 28 under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki and Choi.

The difference, therefore, between claim 28's semiconductor device and the obvious Rai/Tamaki semiconductor device is the former is used in any one of various electronic devices.

Choi teaches that semiconductor devices are conventionally used in various electronic devices (see column 1, lines 10-17).

It would have been further obvious to one skilled in the art to use the obvious Rai/Tamaki semiconductor device in the recited electronic devices because Choi teaches that semiconductor devices are conventionally used in such electronic devices.

Claim 28 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki and Choi.

Claims 29, 30, 34 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 4,004,159 to Rai et al. (Rai) together with United States Patent 5,885,872 to Tamaki et al. (Tamaki, already of record) and United States Patent 5,814,854 to Liu et al (Liu, already of record).

Independent claim 29 parallels independent claim 24 except that claim 29 further recites a NOR type circuit comprising a plurality of transistors. The explanation of the above rejection of claim 24 under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki is thus hereby incorporated by reference into this rejection of claim

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29 under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki and Liu.

The difference, therefore, between independent claim 29 and the obvious Rai/Tamaki device is claim 29 recites a NOR type circuit.

Liu, however, teaches that EEPROM devices are conventionally used to form NOR type circuits (see column 4, lines 1-16).

It would have been further obvious to one skilled in the art use the obvious Rai/Tamaki EEPROM device in a NOR type circuit because Liu teaches that EEPROM devices are conventionally used to form a NOR type circuit.

Claim 29 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki and Liu.

As to dependent claim 30, Tamaki's impurity regions 9 have a striped shape.

Claim 30 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki and Liu.

Independent claim 34 parallels independent claim 24 except that claim 34 further recites a NAND type circuit comprising a plurality of transistors. The explanation of the above rejection of claim 24 under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki is thus hereby incorporated by reference into this rejection of claim 34 under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki and Liu.

The difference, therefore, between independent claim 34 and the obvious Rai/Tamaki device is claim 34 recites a NAND type circuit.

Liu, however, teaches that EEPROM devices are conventionally used to form NAND type circuits (see column 4, lines 1-16).

It would have been further obvious to one skilled in the art use the obvious Rai/Tamaki EEPROM device in a NAND type circuit because Liu teaches that EEPROM devices are conventionally used to form a NAND type circuit.

Claim 34 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki and Liu.

As to dependent claim 35, Tamaki's impurity regions 9 have a striped shape.

Claim 35 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki and Liu.

Claims 33 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over United States Patent 4,004,159 to Rai et al. (Rai) together with United States Patent 5,885,872 to Tamaki et al. (Tamaki, already of record), United States Patent 5,814,854 to Liu et al (Liu, already of record) and United States Patent 5,936,887 to Choi et al. (Choi).

Claims 33 and 38 on independent claims 29 and 34, respectively, which are rejected under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki and Liu (see above). The above explanation of the rejection of independent claims 29 and 34 under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki and Liu is hereby incorporated by reference into this rejection of dependent claims 33 and 38 under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki, Liu and Choi.



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The difference, therefore, between the claims 33 and 38 semiconductor devices and the obvious Rai/Tamaki/Liu semiconductor device is the former are used in any one of various electronic devices.

Choi teaches that semiconductor devices are conventionally used in various electronic devices (see column 1, lines 10-17).

It would have been further obvious to one skilled in the art to use the obvious Rai/Tamaki/Liu semiconductor device in the recited electronic devices because Choi teaches that semiconductor devices are conventionally used in such electronic devices.

Claims 33 and 38 are thus rejected under 35 U.S.C. 103(a) as being unpatentable over Rai together with Tamaki, Liu and Choi.

Claims 39, 41, 43, 44, 46, 48, 49, 51, 53, 57-65, 69-84 and 87 are allowable over the prior art of record.

Claim 86 would be allowable over the prior art of record if corrected.

The applicant's arguments are moot in view of the new grounds of rejection.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

  
Mark V. Prenty  
Primary Examiner